CLAIMS

What is claimed is:

1. A method of controlling timing of synchronization messages between a subscriber access unit and a base station processor in a wireless CDMA system comprising:

providing at least one link between the subscriber access unit and the base station processor, the link establishing a synchronization between the subscriber access unit and the base station processor;

transmitting a synchronization maintenance message from the subscriber access unit to the base station processor; and

computing a timing interval in which to send an additional synchronization maintenance message; the synchronization maintenance messages sufficient to maintain an idling mode connection between the subscriber access unit and the base station processor.

2. The method of claim 1 wherein computing the timing interval further comprises determining a duration required to maintain each of the wireless links.

3. The method of claim 1 wherein the timing interval is a timeslot.

4. The method of claim 3 further comprising a plurality of subscriber access units wherein each of the subscriber access units corresponds to one of a plurality of timeslots.

5. The method of claim 1 wherein the links further comprise active and inactive links and the synchronization maintenance message is transmitted on the inactive links.

6. The method of claim 1 wherein the idling mode connection maintains the synchronization between the subscriber access unit and the base station processor.

7. The method of claim 6 wherein the synchronization further comprises maintaining a code phase lock.

8. The method of claim 7 wherein computing the timing interval further comprises determining a minimal duration for maintaining the idling mode connection.

9. The method of claim 8 wherein the minimal duration is determined using a locking range of the code phase lock circuits at the base station.

10. The method of claim 8 wherein the minimum duration is determined by a channel timing variation.

11. The method of claim 8 wherein the minimum duration is determined by the maximum timing error required to maintain reverse link orthogonality among user channels.

12. The method of claim 1 wherein transmitting the synchronization maintenance message further comprises a timing marker indicative of a reference point for generating timing correction information.

13. The method of claim 12 wherein the timing marker is a pilot symbol.

14. The method of claim 13 wherein the transmitting marker is a short code.

15. The method of claim 1 wherein, in response to the synchronization maintenance message, the base station processor sends an advance/retard message indicative of when the next synchronization maintenance message should be sent.

16. The method of claim 15 wherein the advance/retard message further comprises a link quality management (LQM) timing bit sent on a LQM channel.

17. The method of claim 16 wherein the LQM timing bit corresponds to 1/8 of a chip time.

18. The method of claim 17 wherein after receiving a predetermined number of consecutive identical LQM timing bits, each successive identical LQM timing bit causes timing to be adjusted at an increased rate.

19. The method of claim 18 wherein the predetermined number is eight.

20. A system for controlling timing of synchronization messages between a subscriber access unit and a base station processor in a wireless CDMA system comprising:

a base station processor;

at least one subscriber access unit;

a protocol converter in the base station processor operable to provide at least one wireless link between the subscriber access unit and the base station processor, the wireless link establishing a synchronization between the subscriber access unit and the base station processor; and

a synchronization maintenance message adapted to be sent from the subscriber access unit to the base station processor, the protocol converter further operable to compute a timing interval in which to send an additional synchronization maintenance message, the synchronization maintenance

messages sufficient to maintain an idling mode connection on the wireless link between the subscriber access unit and the base station processor.

21. The system of claim 20 wherein the protocol converter is further operable to determine a duration required to maintain each of the wireless links.

22. The system of claim 21 wherein the timing interval is a timeslot.

23. The system of claim 22 further comprising a plurality of subscriber access units, wherein each of the subscriber access units corresponds to one of a plurality of timeslots.

24. The system of claim 20 wherein the wireless links further comprise active and inactive links and the synchronization maintenance message is transmitted on the inactive links.

25. The system of claim 20 further comprising a plurality of synchronization maintenance messages, wherein the plurality of synchronization maintenance messages maintain the idling mode connection.

26. The system of claim 20 wherein the idling mode connection further comprises maintaining a code phase lock.

27. The system of claim 20 where the protocol converter is further operable to determine a minimal duration for maintaining the idling mode connection.

28. The system of claim 20 further comprising code phase lock circuits having a locking range at the base station, the code phase lock circuits operable to indicate the minimal duration.

29. The system of claim 20 wherein the base station processor is further operable to transmit a timing marker indicative of a reference point for generating timing correction information.

30. The system of claim 29 wherein the timing marker is a pilot symbol.

31. The system of claim 30 wherein the timing marker is a short code.

32. The system of claim 20 wherein the base station processor is further operable to, in response to the synchronization maintenance message, send an advance/retard message indicative of when the next synchronization maintenance message should be sent.

33. The system of claim 31 wherein the advance/retard message further comprises a link quality management (LQM) timing bit sent on an LQM channel.

34. The system of claim 33 wherein the LQM timing bit corresponds to 1/8 of a chip time.

35. The system of claim 33 wherein, after receiving a predetermined number of consecutive identical LQM timing bits, the protocol converter is operable to cause timing to be adjusted at an increased rate upon receiving successive identical LQM timing bit causes.

36. The system of claim 34 wherein the predetermined number is eight.